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Idem

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Description

The following invention relates to a test equipment for providing test signals to stimulate a device under test.

In driver circuits of the type used with automatic test equipment, it is often advantageous to use CMOS integrated chip technology to build the drivers needed to provide the test signal pulses used to stimulate a device under test because of the relative inexpensiveness and compact size of CMOS IC's. The device under test is usually connected to the driver output by a fixed impedance transmission line. Thus, in order to maintain the desired shape of the test pulses, it is necessary to match the output impedance of the driver circuit to the impedance of the transmission line.

One problem with such drivers, however, is that due to performance variations in the CMOS chips, the impedances of such drivers may vary considerably. It is not uncommon for the impedances of similar CMOS devices made by the same manufacturing process to vary as much as 100%. What is needed, therefore, in a test instrument using CMOS transmission gates as output drivers, is a way to match the impedance of each driver to the transmission line which is to be connected to the device under test.

From US-A-3 646 329 an adaptive logic circuit is known which allows selecting weighting constants included in the logic circuit. The logic circuit comprises a voltage divider having a variety of parallel resistances and a common resistance connected in series thereto. The voltage divider gives weighting constants one of which is to be selected by applying outputs of respective stages of a shift register to gates connected between the respective resistances and the common resistance. The output impedance is determined by the resistances of the voltage divider.

From DE-A-32 44 843 an electronically adjustable load for testing power supplies is known. The load comprises a plurality of load transistors to be connected in parallel to the output of the power supply. Each of the load transistors being dimensioned to conduct a predetermined current out of a set of binary-stepped currents when turned on.

It is a principal object of this invention to provide a test equipment having a compact, low-cost driver matching the impedance of a transmission line or other connecting link coupled to a device under test.

The invention is based on a test equipment comprising driver means providing a test signal in response to an actuating signal and a transmission line connected to the driver means for coupling the test signal to a device under test and is characterized in that said driver means is an adjustable impedance driver network which comprises:
a voltage source,
a plurality of transmission gates connected in parallel between the voltage source and the transmission line, each transmission gate having a predetermined nominal impedance when turned on and a substantially infinite impedance when turned off, and
logic circuit means coupled to a control electrode of each of the transmission gates and being responsive to both said actuating signal and a predetermined digital code for selectively turning on various ones of the transmission gates simultaneously, said digital code being determined to provide an impedance for the voltage source matching the impedance of the transmission line.

Thus, the present invention allows matching the impedance of the driver network to the impedance of a transmission line or other connecting link between a test instrument and the device under test. Since the transmission gates are connected in parallel and may be selectively actuated by control signals according to the predetermined digital code, selected ones of the gates may be turned off or turned on to achieve a desired overall impedance for the network.

The gates may be transmission gates utilizing a CMOS FET pair comprising an N channel device and a P channel device connected in parallel. Each gate has a predetermined nominal impedance, and the gates may be related in a binary sense such that for any given plurality of gates connected in parallel, the impedances may be R, 2R, ...2^nR, respectively. Each transmission gate may be controlled by a control line connected to a logic circuit which selectively actuates one or more of the gates in parallel. By turning on various ones of the gates and turning off others, the impedance of the network connecting a voltage source to the transmission line may be controlled.

The foregoing and other objectives, features and advantages of the present invention will be more readily understood upon consideration of the following detailed description of the invention taken in conjunction with the accompanying drawings. In the drawings

FIG. 1 is a block schematic diagram of a variable impedance driver network constructed according to the present invention.

FIG. 2 is a schematic diagram of one of the transmission gates shown in FIG. 1.

A driver network 10 comprises a plurality of CMOS transmission gates 12, 14, 16, 18, 20 and 22. Referring to FIG. 2, which illustrates transmission gate 12, it can be seen that each of the gates 12, 14, 16, 18, 20 and 22 comprises a P channel transistor connected in parallel with an N channel transistor. Both transistors accordingly have a common source 24 and a common drain 26. The gate of the P channel transistor 28 is connected to control line 30 through inverting amplifier 32. Each of the transmission gates 12, 14, 16, 18, 20 and 22, respectively, are controlled by control lines 30, 34, 36, 38, 40 and 42, respectively. The state of each of the control lines 30, 34, 36, 38, 40 and 42 are controlled by coded input lines C1, C2, C3, C4, C5 and C6 in conjunction with lines A1 and A2 which control the state of the driver 10, that is whether it is to be in a high or low level logic state.

The output of the driver 10 is connected to a transmission line 44 which in turn may be connected to a device under test 46. By controlling various ones of the transmission gates 12, 14 and 16 in, for example, a high level logic state, one may choose the output impedance of the driver circuit 10. This is because each of the transmission gates 12, 14 and 16 has a predetermined nominal impedance when turned on and has a nearly infinite impedance when turned off. Thus, by selectively turning on and off various ones of the transmission gates, the overall impedance, which is calculated according to Ohm's Law, may be adjusted.

A finer degree of adjustment may be provided if the individual impedances of the transmission gates in their "on" states are binarily related. That is, if gate 12 has a resistance R, gate 14 would have a resistance 2R and gate 16 would have a resistance 4R. There may be more than three gates for the high and low logic levels respectively, and in such a case the values of the resistances would be R, 2R, ...2^nR, respectively. Thus, the high control line A1 or the low control line A2 controls whether the driver is in a high or a low logic states, and combinations of the control lines C1 through C3 for the high voltage level and C4 through C6 for the low voltage level control the output impedance of the driver 10 according to a digital code which selectively enables various ones of the transmission gates 12, 14, 16, 18, 20 and 22.

The terms and expressions which have been employed in the foregoing specification are used therein as terms of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding equivalents of the features shown and described or portions thereof, it being recognized that the scope of the invention is defined and limited only by the claims which follow.

Claims

1. A test equipment comprising:
   driv r means (12-22) providing a test signal in response to an actuating signal (A1, A2) and a transmission line (44) connected to the driver m ans (12-22) for coupling the test signal to a device under test (46),
   characterized in that
   said driver means (12-22) is an adjustable impedance driver network which comprises:
   - a voltage source,
   - a plurality of transmission gates (12-22) connected in parallel between the voltage source and the transmission line (44), each transmission gate (12-22) having a predetermined nominal impedance when turned on and a substantially infinite impedance when turned off and
   - logic circuit means coupled to a control electrode (30, 34-42) of each of the transmission gates (12-22) and being responsive to both said actuating signal (A1, A2) and a predetermined digital code (C1-C6) for selectively turning on various ones of the transmission gates (12-22) simultaneously, said digital code (C1-C6) being determined to provide an impedance for the voltage source matching the impedance of the transmission line (44).

2. A test equipment as recited in claim 1, characterized in that the logic circuit means comprises an AND gate array, each AND gate having an output coupled to each respective control electrode (30, 32-42) and having inputs receiving the actuating signal (A1, A2) and one bit of the digital code (C1-C6).

3. A test equipment as recited in claim 1, characterized in that the nominal impedances of the transmission gates (12-22) are R, 2R, ..., 2^nR, respectively, where n is the total number of transmission gates (12-22) minus one.

4. A test equipment as recited in claim 1, characterized in that the voltage source includes a high level voltage source and a low level voltage source, with a first half (12-16) of the transmission gates connected between the high level voltage source and the transmission line (44) and with a second half (18-22) of the transmission gates connected between the low level voltage source and the transmission line (44).

5. A test equipment as recited in claims 1 or 4, characterized in that each transmission gate (12-22) is a pair of CMOS field effect transistors of opposite polarity connected togeth r in parallel with its sources (24) connected to the voltage source and its drains (26) connected to the transmission line (44), and in that the con-

trol signal (A1, A2) and an inverted control signal each from the logic circuit means is coupled to each control gate (28) of said pair of CMOS field effect transistors, respectively.

6. A test equipment as recited in claim 4, characterized in that the logic circuit means comprises an AND gate array having a first and a second portion, each AND gate of the first portion having an output coupled to each respective control electrode (30, 34, 36) of the first half (12-16) of the transmission gates and having inputs including a first bit (A1) of the actuating signal for selecting the high level voltage source and one bit of the digital code (C1-C3), and each AND gate of the second portion having an output coupled to each respective control electrode (38-42) of the second half (18-22) of the transmission gates and having inputs including a second bit (A2) of the actuating signal and one bit of the digital code (C4-C6).

7. A test equipment as recited in claim 4, characterized in that the nominal impedances for each half of the transmission gates (12-22) are R, 2R, ..., 2^nR, respectively, where n is the total number of transmission gates (12-22) per half minus one.

Patentansprüche

1. Testgerät mit

einer Treiberschaltung (12 bis 22), die in Abhängigkeit von einem Betätigungssignal (A1, A2) ein Testsignal erzeugt, und mit einer mit der Treiberschaltung (12 bis 22) verbundenen Übertragungsleitung (44) zur Kopplung des Testsignals auf eine zu testende Anordnung,

dadurch gekennzeichnet, daß

die Treiberschaltung (12 bis 22) ein Treibernetzwerk mit einstellbarer Impedanz und mit folgenden Komponenten ist:

eine Spannungsquelle,

eine Vielzahl von zwischen der Spannungsquelle und der Übertragungsleitung (44) parallelgeschalteten Übertragungsgattern (12 bis 22), die jeweils eine vorgegebene Nenn-Impedanz im eingeschalteten Zustand und eine im wesentlichen unendlich große Impedanz im ausgeschalteten Zustand besitzen, und

eine an jeweils eine Steuerelektrode (30, 34 bis 42) der Übertragungsgatter (12 bis 22) angekoppelte und sowohl vom Betätigungssignal (A1, A2) und einem vorgegebenen Digitalcode angesteuerte Logikschaltung zur gleichzeitigen Einschaltung mehrerer Übertragungsgatter, wobei der Digitalcode so festgelegt ist, daß er eine an die Impedanz der Übertragungsleitung (44) angepaßte Impedanz für die Spannungsquelle erzeugt.

2. Testgerät nach Anspruch 1, **dadurch gekennzeichnet**, daß die Logikschaltung ein UND-Gatterfeld umfaßt, in dem die UND-Gatter jeweils einen an eine entsprechende Steuerelektrode (30, 32 bis 42) gekoppelten Ausgang und jeweils das Betätigungssignal (A1, A2) und ein Bit des digitalen Codes (C1 bis C6) aufnehmende Eingänge besitzen.

3. Testgerät nach Anspruch 1, **dadurch gekennzeichnet**, daß die Nenn-Impedanzen der Übertragungsgatter (12 bis 22) gleich R, 2R, ..., bzw. 2^nR sind, worin n die Gesamtanzahl der Übertragungsgatter (12 bis 22) minus Eins ist.

4. Testgerät nach Anspruch 1, **dadurch gekennzeichnet**, daß die Spannungsquelle eine Hochspannungsquelle und eine Niederspannungsquelle enthält und daß die erste Hälfte (12 bis 16) der Übertragungsgatter zwischen die Hochspannungsquelle und die Übertragungsleitung (44) und die zweite Hälfte (18 bis 22) der Übertragungsgatter zwischen die Niederspannungsquelle und die Übertragungsleitung (44) geschaltet ist.

5. Testgerät nach Anspruch 1 oder 4, **dadurch gekennzeichnet**, daß die Übertragungsgatter jeweils durch ein Paar von parallelgeschalteten CMOS-Feldeffekttransistoren entgegengesetzten Leitungstyps gebildet sind, deren Source (24) mit der Spannungsquelle und deren Drain (26) mit der Übertragungsleitung (44) verbunden sind, und daß das Steuersignal (A1, A2) sowie ein invertiertes Steuersignal von der Logikschaltung auf die Steuergates (28) des jeweiligen Paars von CMOS-Feldeffekttransistoren gekoppelt sind.

6. Testgerät nach Anspruch 4, **dadurch gekennzeichnet**, daß die Logikschaltung ein UND-Gatterfeld mit einem ersten und einem zweiten Teil umfaßt, daß die UND-Gatter des ersten Teils jeweils mit einem Ausgang an eine entsprechende Steuerelektrode (30, 34, 36) der ersten Hälfte (12 bis 16) der Übertragungsgatter gekoppelt sind, das Eingangssignale für die UND-Gatter des ersten Teils ein erstes Bit (A1)

des B tätigungssignals zur Auswahl der Hochspannungsquelle und ein Bit des Digitalcodes (C1 bis C3) umfassen und daß die UND-Gatter des zweiten Teils mit ihrem Ausgang jeweils an eine entsprechende Steuerelektrode (38 bis 42) der zweiten Hälfte (18 bis 22) der Übertragungsgatter gekoppelt sind und Eingangssignale für die UND-Gatter des zweiten Teils ein zweites Bit (A2) des Betätigungssignals und ein Bit des Digitalcodes (C4 bis C6) umfassen.

7. Testgerät nach Anspruch 4, **dadurch gekennzeichnet**, daß die Nenn-Impedanzen für jede Hälfte der Übertragungsgatter (12 bis 22) gleich R, 2R, ..., bzw. 2^nR sind, worin n die Gesamtzahl der Übertragungsgatter (12 bis 22) pro Hälfte minus Eins ist.

Revendications

1. Equipement de test comprenant :
   un moyen de pilotage (12-22) qui produit un signal de test en réponse à un signal d'actionnement (A1, A2) et une ligne de transmission (44) qui est connectée au moyen de pilotage (12-22) pour coupler le signal de test à un dispositif en cours de test (46) ;
   caractérisé en ce que :
   ledit moyen de pilotage (12-22) est un réseau de dispositif de pilotage à impédance réglable qui comprend :
   une source de tension ;
   une pluralité de portes de transmission (12-22) connectées en parallèle entre la source de tension et la ligne de transmission (44), chaque porte de transmission (12-22) présentant une impédance nominale prédéterminée lorsqu'elle est rendue passante et une impédance sensiblement infinie lorsqu'elle est rendue bloquée ; et
   un moyen de circuit logique qui est couplé à une électrode de commande (30, 34-42) de chacune des portes de transmission (12-22) et qui est sensible à la fois audit signal d'actionnement (A1, A2) et à un code numérique prédéterminé (C1-C6) pour rendre passantes de façon sélective et simultanément certaines portes de transmission prises parmi les portes de transmission (12-22), ledit code numérique (C1-C6) étant déterminé pour produire une impédance pour la source de tension qui s'adapte à l'impédance de la ligne de transmission (44).

2. Equipement de test selon la revendication 1, caractérisé en ce que le moyen de circuit logique comprend un réseau de portes ET, chaque port ET comportant une sortie qui est couplée à chaque électrod de commande respective (30, 32-42) et comportant des entrées qui reçoivent le signal d'actionnement (A1, A2) et un bit du code numérique (C1-C6).

3. Equipement de test selon la revendication 1, caractérisé en ce que les impédances nominales des portes de transmission (12-22) sont respectivement R, 2R,..., 2^nR, où n est le nombre total de portes de transmission (12-22) moins un.

4. Equipement de test selon la revendication 1, caractérisé en ce que la source de tension inclut une source de tension de niveau haut et une source de tension de niveau bas, une première moitié (12-16) des portes de transmission étant connectée entre la source de tension de niveau haut et la ligne de transmission (44) et une seconde moitié (18-22) des portes de transmission étant connectée entre la source de tension de niveau bas et la ligne de transmission (44).

5. Equipement de test selon la revendication 1 ou 4, caractérisé en ce que chaque porte de transmission (12-22) est une paire de transistors à effet de champ CMOS (métal-oxyde-semiconducteur complémentaires) de polarités opposées qui sont connectés ensemble en parallèle, leurs sources (24) étant connectées à la source de tension et leurs drains (26) étant connectés à la ligne de transmission (44) et en ce que le signal de commande (A1, A2) et un signal de commande inversé, chacun provenant du moyen de circuit logique, sont respectivement couplés à chaque porte de commande (28) de ladite paire de transistors à effet de champ CMOS.

6. Equipement de test selon la revendication 4, caractérisé en ce que le moyen de circuit logique comprend un réseau de portes ET qui comporte une première et une seconde parties, chaque porte ET de la première partie comportant une sortie couplée à chaque électrode de commande respective (30, 34, 36) de la première moitié (12-16) des portes de transmission et comportant des entrées qui incluent un premier bit (A1) du signal d'actionnement pour sélectionner la source de tension de niveau haut et un bit du code numérique (C1-C3), et chaque porte ET de la seconde partie comportant une sortie qui est couplée à chaque électrode de commande respective (38-42) de la seconde moitié (18-22) des portes de transmission et comportant des entrées qui incluent un second bit (A2) du signal d'action-

nement et un bit du code numérique (C4-C6).

7. Equipement de test selon la revendication 4, caractérisé en ce que les impédances nominales pour chaque moitié des portes de transmission (12-22) sont respectivement A, 2R,..., 2^nR, où n est le nombre total des portes de transmission (12-22) par moitié moins un.

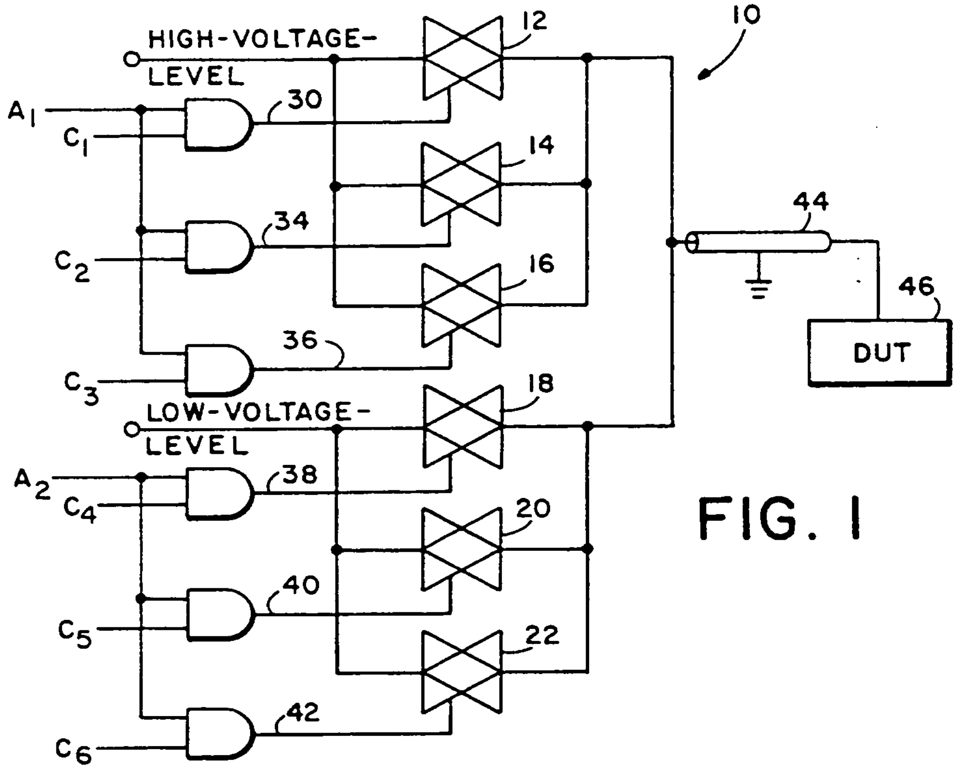

FIG. 1

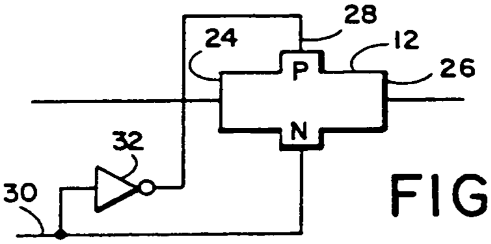

FIG. 2

TRANSMISSION GATE

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Applic. #

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